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A REVIEW ARTICLE OF MULTILEVEL INVERTER CONFRIGURATION 4 POLE INDUCTION MOTOR WITH SINGLE DC LINK

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ABSTRACT

A new simplified space vector PWM method for a three-level inverter is proposed in this proposed work. The three level inverter has a large number of switching states compared to a two- level inverter. In the proposed scheme, three-level space vector PWM inverter is easily implemented than as conventional two-level space vector PWM inverter. This Technique presents a novel DC link balancing scheme for a back-to-back system with three-level diode clamped topologies. The proposed algorithm is improvement of the variable switching frequency control strategy formerly introduced with the three level back-to-back system and it relays on measurement of adjacent capacitor voltages which provide information about the potential variation in consecutive nodes of the three-level DC link network, Therefore, the proposed method can also be applied to multilevel inverters. In this work, a three-level inverter using space vector modulation strategy has been modeled and simulated.

I. INTRODUCTION

Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them [1-2]. The output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion. In recent years, beside multilevel inverters various pulse width modulation (PWM) techniques have been also developed. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available as compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states.

One of the advantages of multilevel inverters is that the voltage stress on each switching device is reduced. In addition, multilevel waveforms feature have less harmonic content compared to two level waveforms operating at the same switching frequency. In this paper, modeling and simulation of a multilevel inverter using cascaded inverters with separated DC sources have been performed with R-L load using Simulink/ MATLAB package program. In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverters. Minimum level number of a multilevel inverter is three and three-level inverter structure is chosen in this work.

II. MULTILEVEL CONCEPT

This paragraph has the aim to introduce to the general principle of multilevel behavior. Considering Figure 1. the voltage output of a 3-level inverter leg can assume three values: 0 , E or 2E . In Figure 1.generalized n-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, and then the voltage levels can be different. This

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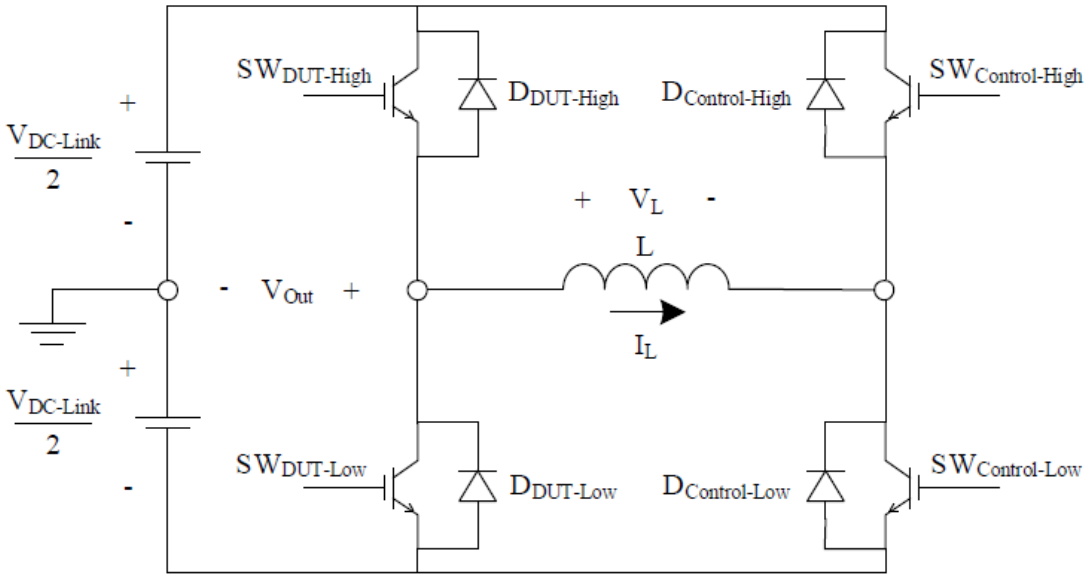
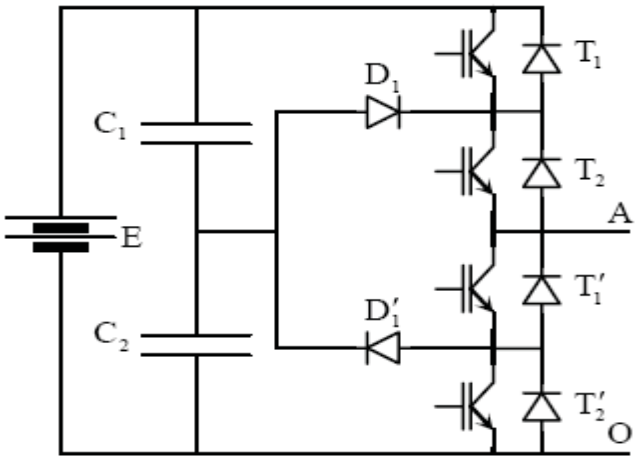
introduces a further possibility which can be useful in multiphase inverters, as it will be shown in the following. A three-phase inverter composed by n-level legs will be considered for the analysis.



Fig(1) Single DC link.

III. DIODE-CLAMPED OPERATING PRINCIPLE

3-level diode-clamped leg is shown it is easy to extend the scheme to a generic n-level configuration. The DC bus voltage is split in two and four equal steps respectively by capacitor banks. In this way, no extra DC sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called clamping diodes. Anyway, to better understand how a diode-clamped works, it is preferred to use series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor.



Fig(2) Diode-clamped circuit.

IV. POWER CIRCUIT DESIGN

The power circuit designed contains full bridge rectifier with DC Link filter, full bridge inverter assembly and LCR filter assembly. At the start of the motor it experiences a very high current and the motor may not run at the rated speed. An electromagnetic relay is used in the proposed scheme. Starting current of the induction

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motor is six times that of the rated current for a duration of 4 Seconds. To limit this heavy current flow, two wire wound resistances of 50Ω, 10W each are connected in parallel to the input supply. A single pole change over relay is used to insert these wire wound resistors for a period of 4secs and then the relay bypasses these resistors for the rest of the operation.

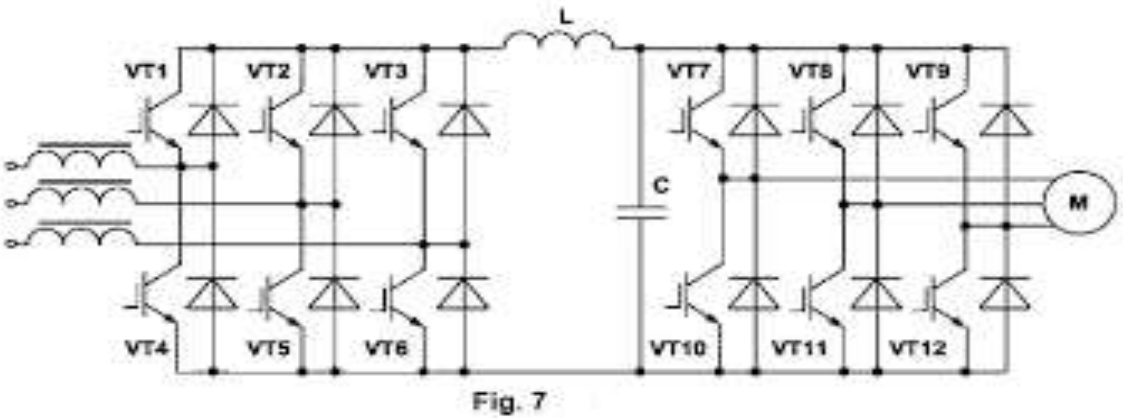

Fig (3) power circuit

V. CONTROL CIRCUIT

The control circuit of the proposed scheme consists of a Digital signal Controller dsPIC30F2010.A Digital Signal Controller (DSC) is a single-chip, embedded controller that seamlessly integrates the control attributes of a Microcontroller (MCU) with the computation and throughput capabilities of a Digital Signal Processor (DSP) in a single core. The dsPIC DSC has the "heart" of a 16-bit MCU with robust peripherals and fast interrupt handling capability and the "brain" of a DSP that manages high computation activities, creating the optimum single-chip solution for embedded system designs. The dsPIC30F devices contain extensive Digital Signal Processor (DSP) functionality within high-performance 16-bit microcontroller (MCU) architecture. It also consists of six opto-coupler for isolating the control and power circuits. In this work an opto-coupler TLP250 is used to isolate the gate drive circuit and the IGBT-based power circuit Six IGBTs of the power circuit are controlled by the PWM signals generated by the control circuit.

VI. SELECTION OF SWITCHING VECTORS

Given a reference vector, there are numerous ways to synthesize it using different vectors. For example, it can be synthesized using 81, 82, and 8Z1 and/or 8Z2; or using. It is proven that by using the adjacent non-zero vectors, which defines each sector, and the zero vectors, the circulating energy is minimized. The current ripple and harmonic contents would also be reduced. Therefore, this is the most favorable way to select the switching vectors. It is sometimes called six-step space vector modulation. However, non-six-step space vector modulations are also useful for transient in that a faster regulation can be achieved, and for some special cases where zero vectors cannot be used [B19] [D1].

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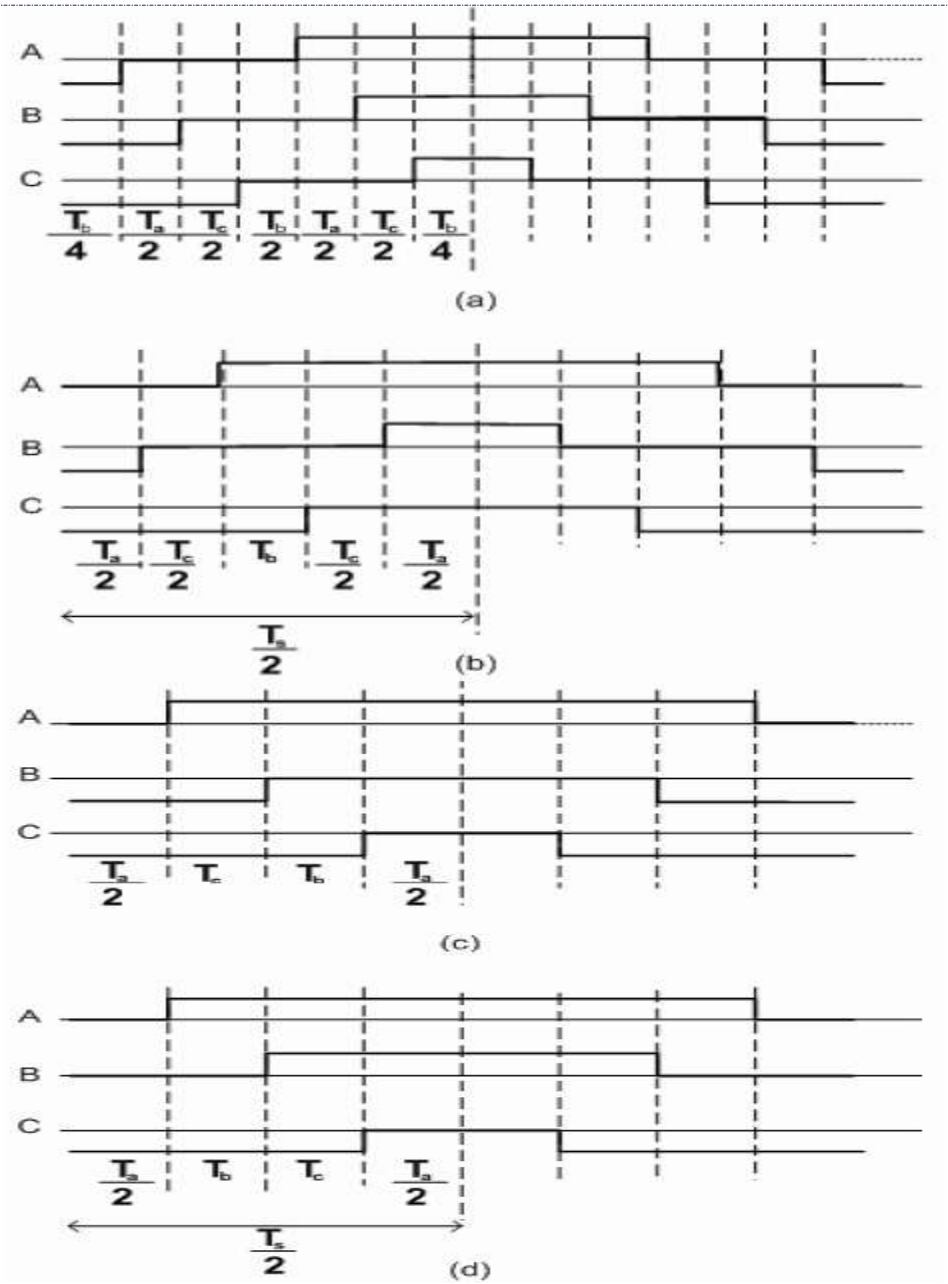

Fig(4) Switching controlling

VII. OVER-MODULATION IN A-B-G COORDINATES

Over-modulation happens in the following situations:

(1) Large transient;
(2) Highly unbalance;
(3) Highly nonlinear;
(4) Fault mode operation.

When the reference vector is outside the region confined by the surfaces given byte 24 tetrahedrons, the three-dimensional space vector modulation goes into over-modulation mode. The duty ratios of switching vectors may become negative values if the reference vector is not modified. The over-modulation mode for the three-dimensional SVM is similar to the two-dimensional version. Instead of the hexagon in the two-dimensional case, there are three over-modulation surfaces in each prism. The over-modulation surfaces confine the attainable region. The example of the three over-modulation surfaces in prism I is shown in Figure 3-34. When

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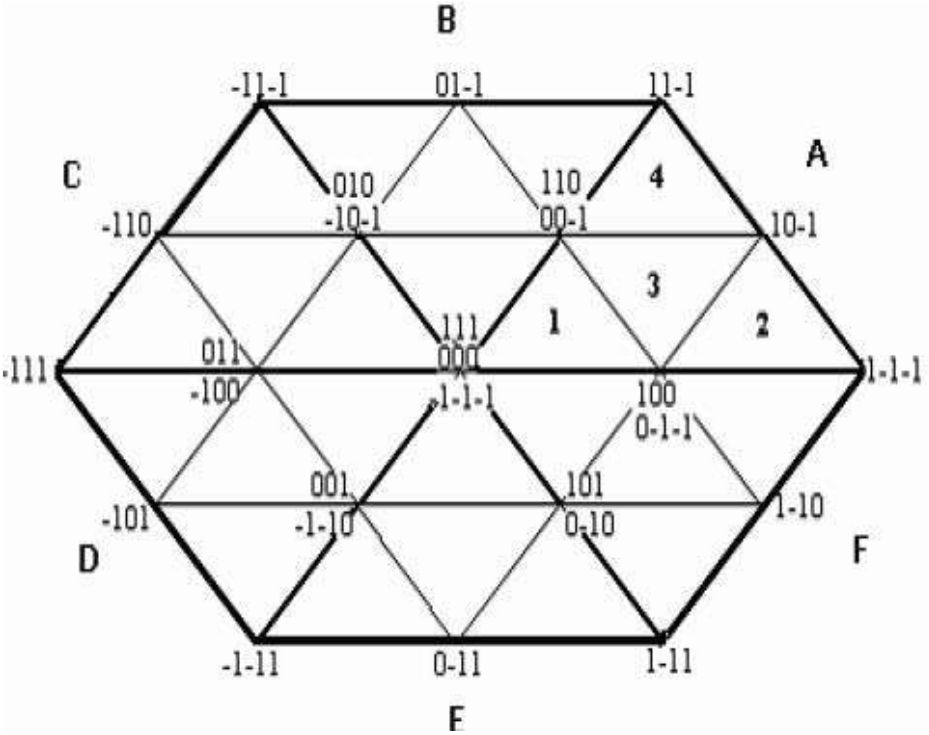
the reference vector intersects with any of the three over-modulation surfaces, the reference vector is modified to the intersection point on that over-modulation surface.

VIII. VERIFICATION OF MODEL FOR FOUR-LEGGED INVERTER

In order to verify the validity of the developed small-signal model of the four legged inverter, the setup shown in Figure 4-6 has been used to measure the open loop control-to-output-voltage transfer functions. The impedance analyzer HP 4194A outputs perturbation signal sweeping from 20 Hz to 2 kHz. The analog perturbation signal is fed to the reference channel of the impedance analyzer, and is also converted to a digital signal at a sampling frequency of 5 kHz. The system is perturbed by adding this digitized perturbation to the steady-state duty ratio in a digital signal processor (DSP). The output voltages are measured and then transformed into the d-q-o coordinate. The output voltages in d-q-o coordinate are then converted back to analog signal at a sampling rate.

IX. MODELING AND CONTROL OF FOUR-LEGGED ONVERTERS IN D-Q-O ROTATING COORDINATE

In this chapter, average large signal models of four-legged voltage source inverter and PFC rectifier in the d-q-o rotating coordinate are given. Small signal models are derived by perturbing the large signal models at the operating point. Control loop designs based on the small signal models are performed. The unbalanced and nonlinear loads are also modeled in the d-q-o coordinate, which makes clear the challenges the control design faces when the load is unbalanced and/or nonlinear. Simulation and experimental results show performance of the four-legged voltage source inverter under different load conditions with the voltage loop closed. The fault tolerant operation of the four-legged PWM rectifier is demonstrated by simulation results.



V_{x0}	S_{X1}	S_{X2}	S_{X1}'	S_{X2}'
$V_{dc}/2$	1	0	0	1
0	1	1	0	0
0	0	1	0	1
$-V_{dc}/2$	0	1	1	0

Fig(5) Tabulated Output.

The principle of SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors obtained by vector calculations; where V1, V2, and V3 are vectors that define the triangle region in which V* is located. T1, T2 and T3 are the corresponding vector durations and Ts is the sampling time. In a three-level inverter similar to a two-level inverter, each space vector diagram divided into 6 sectors. For simplicity here only the switching patterns for Sector A will be defined so that calculation technique for the other sectors will be similar. Sector A is divided into 4 regions as shown in Fig.3 where all the possible switching states for each region are given as well.

SVPWM for three-level inverters can be implemented by considering the following steps;

1. Determine the sector,
2. Determine the region in the sector,
3. Calculate the switching times, Ta, Tb, Tc
4. Find the switching states.

X. CONCLUSION

Design of DC link filter and inverter output filter for three phase induction motor drive system has been presented. The developed hardware setup is tested on a three phase 1.5hp, 415V, 50Hz induction motor with loading in power electronics laboratory. The harmonic contents at the output were studied on the storage oscilloscope. We found that the designed filters effectively reduced the harmonic distortions. From the experimental setup and results chapter it is observed that by the use of the designed filter at the rectifier and at the output of the inverter, almost a pure sinusoidal supply is given to the motor drive system, with this the operation of closed loop control system becomes very smooth and the torque pulsation will be reduced to the maximum extent. With this we can say that efficiency of the overall system is increased.

Advantages of the Design of DC link filter and inverter output filter for three phase induction motor drive system are: Reduction in harmonics, improved life of the motor, high efficiency, high power factor. There are various application areas for harmonic filters, the most important being: Adjustable speed drives, Computer Equipments, Welders and Battery charges.

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